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DC Fault Isolation Study of Bidirectional Dual Active Bridge DC/DC Converter for DC Transmission Grid Application

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Abstract— **Fast isolation and detection of DC faults is currently a limiting factor in high power DC transmission grid development. Recent research has shown that the role of DC/DC converters is becoming increasingly important in solving various DC grid challenges such as voltage stepping, galvanic isolation and power regulation. This paper focuses on an additional important feature of bidirectional dual active bridge (DAB) DC-DC converters which make it attractive for future DC grids; it's inherent fault isolation capability which does not need control intervention to limit fault current in case of the most severe DC faults. Detailed analytical, simulation and experimental study are performed by subjecting the converter to DC short circuit faults at its DC voltage terminals. The results obtained have shown significant advantage of DAB where fault current is less than rated current during the fault duration. Thus no control action is necessary from the non-faulted bridge to limit fault current and no external DC circuit breakers are required. This advantage makes DAB converter feasible for DC grid integration.**

***Keywords*- DC-DC converter, Dual active bridge (DAB) converter, DC fault, voltage source converter (VSC).**

I. INTRODUCTION

High/medium power DC-DC converters are expected to play a significant role in multi-terminal high voltage direct current transmission (HVDC) based DC grids. Among these functionalities are DC voltage stepping, power regulation, interconnection of different DC systems, DC line tapping, fault detection and isolation [1]. In a DC grid, a DC-DC converter should have characteristics of a high voltage stepping and DC fault ride through capability whilst been cost effective.

One of the most significant issues in DC grid development for the last decade has been fast isolation and detection of DC fault currents. This is due to DC fault susceptibility of voltage source converters (VSC) in HVDC transmissions [2]. In the event of DC fault at the converter terminals or along the DC line, the VSC converter functions as uncontrolled rectifier diode, thereby resulting in unacceptable level of fault current flowing through the freewheeling diodes, even when all the IGBTs are switched off. This is worsened further due to the non-zero crossing points of DC current, low impedance of the DC cables, wave propagation delay leading to steep rise of the fault current magnitude and delay in selective fault current isolation [3]; which might result in destruction of the converter switches. It is not acceptable to shut down the entire grid when a fault occurs, hence to preserve the grid integrity and security, a robust fault protection mechanism that will respond in a very short time in the event of DC fault is paramount to protect DC-DC converters or a DC-DC converters that have DC fault isolation characteristics along the DC line are required.

Different fault protection technologies for DC grid have extensively been studied in literature to overcome the effect of overvoltage and currents. Conventional mechanical AC circuit breaker at the VSC terminals [4,5], is inexpensive approach but unsuitable for clearing DC faults due to slow response time, thus exposing the VSC converter switches to high fault current in the process. Solid state DC circuit breakers [3,5] can isolate the fault rapidly by providing fast breaking time, but it's expensive and results in high on state losses due semiconductors in the current path. In [4, 6], a hybrid circuit breakers using a solid state and mechanical breakers that can achieve fast fault isolation has been demonstrated. But the breakers have a large foot print; higher cost and no comprehensive test data is available in DC grid environment. Fault current limiting using superconducting fault current limiters [7, 8], is another approach discussed in literature. But the limiter fault current varies with the condition of the AC grid and the location of the fault along the line [9].

Fault current isolation at VSC level for both two level and modular multilevel (MMC) VSC converters with fault current blocking capability is undergoing extensive research [2,10,11]. [10, 11], presented MMC converters with DC reverse blocking capability. But with both two level and MMC based VSC converters, a high magnitude inrush current stress is experienced by the switches when the fault is cleared due uncontrolled instant charging of the long DC cables [2]. A hybrid cascaded MMC converter is addressed in [2], that can reduce the extreme inrush currents, provide AC and DC fault ride through, but at significant capital cost and large foot print due to additional AC side cascaded full bridge chain links.

DC-DC converters have been proposed as a solution to address DC fault currents problem, besides its voltage stepping and power regulation functionalities in the grid. In [12] a high power converter thyristor based switches was analysed. Even though the converter achieves a fault isolation and moderate stepping ratios, lack of galvanic isolation and low efficiency at high stepping ratios are its drawbacks. In [13], an IGBT based LCL resonant converter was studied that

addressed some of the limitations of converter [12] but without isolation between the two bridges. An MMC DC-DC converter based on the concept of DC transformer is suggested in [14] that achieve DC blocking, but at the expense of large number of components and increased losses.

This paper focuses on one important feature of bidirectional dual active bridge (DAB) DC-DC converter [15]: its inherent fault isolation capability without a need for a very fast controller to limit fault current. Among DAB converter desirable features making them a suitable candidate for DC grids are low number of passive components (only a single series inductor/transformer), galvanic isolation, low switching losses, fast power reversal, high power density, buck/boost operation and possibility of high stepping ratio of conversion. However, there is no detail study of fault response characteristics of the converter in a DC grid environment and thus, DAB converter fault interruption characteristics, under extreme pole to pole DC faults will be evaluated through analytically, and verified through simulation studies and experimental implementation.

II. DAB CONVERTER DC FAULT ANALYSIS

Bidirectional DAB circuit topology depicted in Fig. 1(a) consists of two H-bridges, external inductor L_{ext}, to facilitate power transfer and isolation transformer. By referring the converter to the transformer primary side, neglecting transformer magnetizing inductance, adding transformer leakage inductance to the external inductor (L_{ext}) to form $L_{tot,}$ and with *n:1* transformer turns ratio, circuit of Fig. 1 (a), can be simplified to its AC equivalent circuit model in Fig.1 (b). DAB under triple phase shift (TPS) control can be used to control both converter bridges independently both for power regulation and fault current control. Three parameters D_1, D_2 and D_3 are used to control the converter bridges. D_1 is the inner phase shift between switches S_1 & S_4, D_2 is the inner phase shift between the switches Q_1 & Q_4 while D_3 is the outer phase shift between S_1 & Q_1 as illustrated in the waveform of Fig. 1(c). All the equations in this section will be based on analysis performed in [16].

Fault study is performed by assuming the converter is operating at full rated power for a worst case scenario. Rated inductor/transformer RMS current can be obtained at maximum DAB power transfer condition (TPS control variables D_1=*1, D2=1* & D_3=*0.5*). From [16], this can be expressed as follows:

$$I_{L(rated\_RMS)} = \frac{1}{4 f_s L_{tot}} \sqrt{\frac{V^2_{DC1} + n^2 V^2_{DC2}}{3}} \tag{1}$$

where

f_s is the converter switching frequency, L_{tot} is the total equivalent interface inductance, n is the transformer turns ratio and V_{DCi} (i=1,2) are the two DC side voltages.

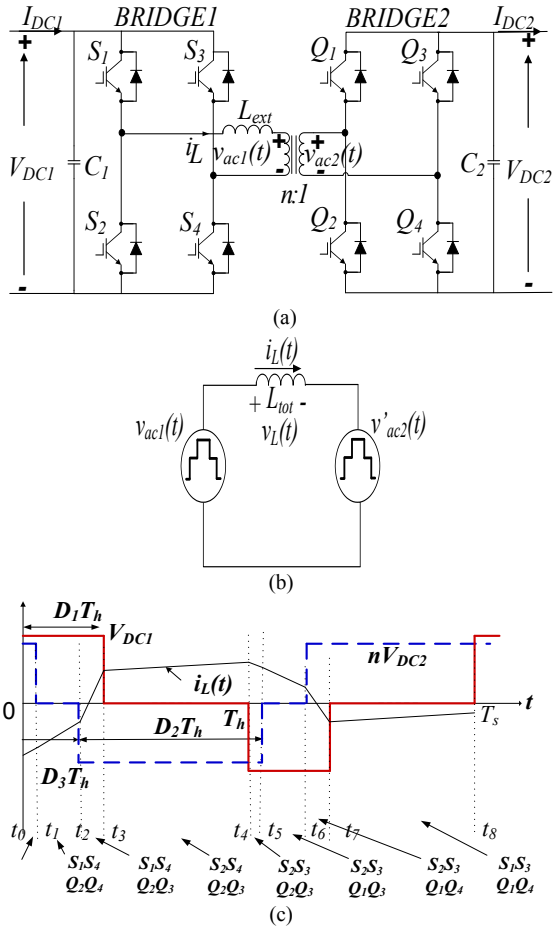


Fig. 1. (a) DAB circuit diagram (b) Simplified model with secondary side of transformer referred to the primary (c) Ideal voltage & current waveforms of TPS control [16].

Fault analysis of the converter is performed by subjecting the converter to a worst case pole to pole DC short circuit fault. Either terminal can be used since analysis is identical. Consider a short circuit at V_{DC2} terminal, the converter is assumed to be transferring full rated power prior to the fault from terminal 1 to terminal 2. Therefore, by substituting V_{DC2}=*0* in (1), the RMS and peak fault currents can be expressed as [16]:

$$I_{L(fault\_RMS)} = \frac{1}{\sqrt{3}} \frac{V_{DC1}}{4 f_s L_{tot}} \tag{2}$$

$$I_{L(rated\_peak)} = I_{L(fault\_peak)} = \frac{V_{DC1}}{4 f_s L_{tot}} \tag{3}$$

From (3), it can be observed that during the fault, the peak current remains unchanged compared to rated peak current. It is common from manufacturers' datasheets to find IGBTs designed to operate at twice the maximum rated current of the converter for a short duration of time (2 *p.u*). By assessing ratio of RMS fault current (2) to RMS rated current (1),

$$\frac{V_{DC1}}{\sqrt{V^2_{DC1} + n^2 V^2_{DC2}}} < 1 \tag{4}$$

Thus, (4) shows that the fault current RMS value is always smaller than full-load current. This demonstrates fault tolerant characteristics of the converter and hence IGBTS of non-faulted side do not need to be tripped to limit fault current. Peak fault current is equal to peak rated current, and RMS fault current is 70.7% of rated RMS current in the most common design case of the DAB converter where the transformer turns ratio n matches the DC side voltage ratios for minimizing current circulation ($n=V_{DC1}/V_{DC2}$). Similarly, by replacing $V_{DC1}=0$ in (1), analytical expressions when fault occurs at V_{DC1} terminal can be obtained yielding the same fault current-to-rated current ratios.

III. SIMULATION RESULTS

In this section, Matlab/Simulink simulation results of the converter will be presented by applying a solid pole to pole short circuit at DC terminals of the converter. A test system illustrated in Fig.2 is used to validate the analytical analysis of previous section using parameters shown in Table I.

A. DC fault on LV side (V_{DC1})

Fig. 3 and Fig. 4, shows the simulations results obtained when short circuit fault is applied at the *24V* DC terminal. The converter is operating at full rated power with bridge 2 sourcing, before the fault is applied at time *t=0.1s* and cleared at *t=0.2s*. Fig. 3 (a) and (b) show the converter AC terminal voltages v_{ac1} and v_{ac2}. It can be observed during the fault period that the voltage reduces on v_{ac1} while v_{ac2} remains unchanged. As waveform of Fig. 3(c) illustrates, the peak inductor/transformer current is nearly constant while there is reduction in RMS current in the fault duration (bold dotted line) to 70% rated current, which confirms the theoretical analysis. This is significant advantage of DAB where fault current is less than rated current due to absence of opposite polarity AC voltages during the fault which increases total resultant voltage across DAB inductor leading to higher currents. Hence, for this reason, no control action is applied from the non-faulted side bridge 2 to limit fault current.

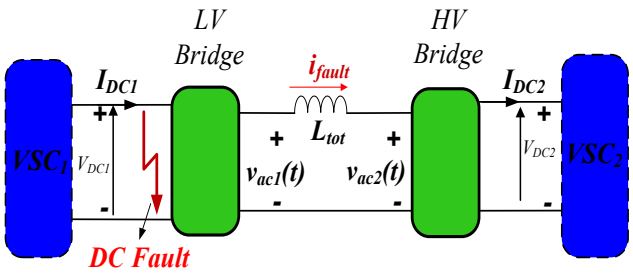
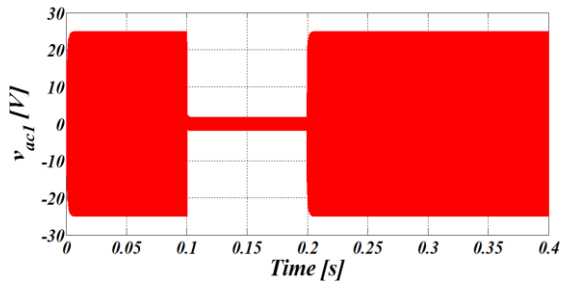


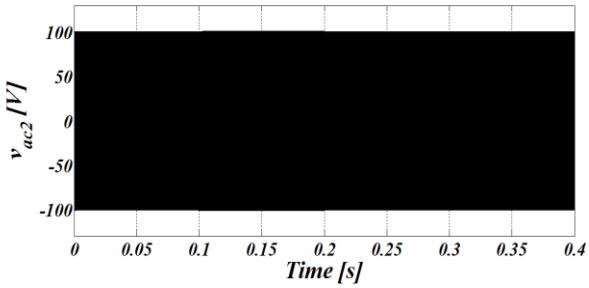
Fig. 2. Test system used for fault analysis

Table I: Summary of converter parameters

Power	V_{DC1}	V_{DC2}	L_{tot}	f_s	*n*
568W	*24V*	*100V*	*63.36uH*	*2kHz*	*24/100*



(a)



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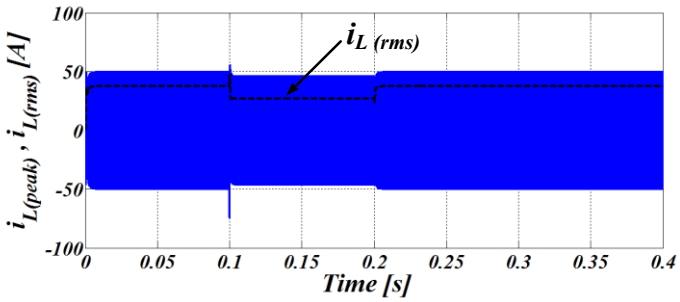
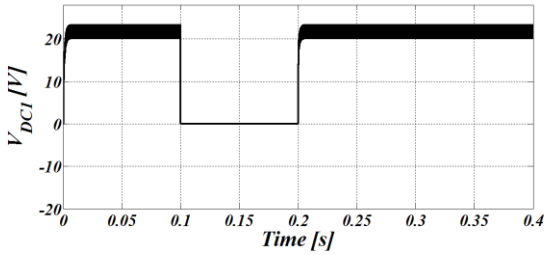
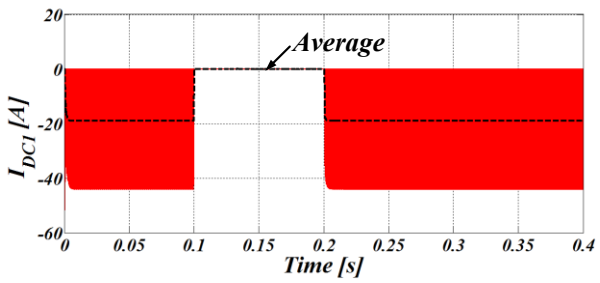


(c)

Fig. 3. Simulation results showing DC fault on LV side (a) Bridge 1 AC voltage v_{ac1}, (b) Bridge 2 AC voltage v_{ac2} , (c) Inductor current i_L.



(a)



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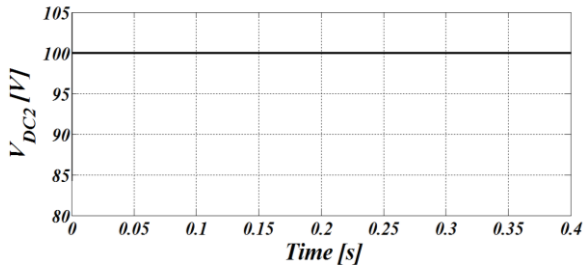

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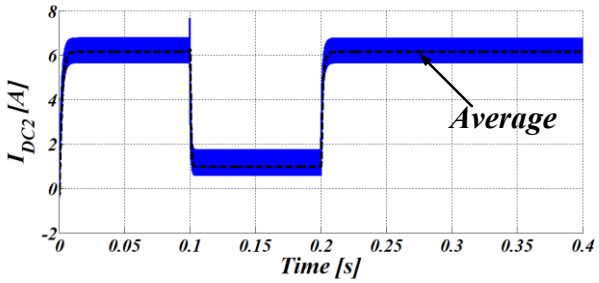


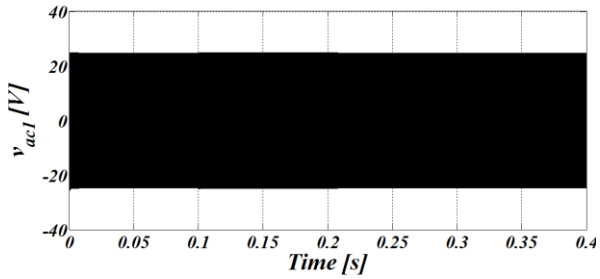
(d)

Fig. 4. Simulation results for DC voltages and currents for DC fault on LV side *(a)* Terminal 1 DC voltage V_{DC1}, (b) Terminal 1 DC current I_{DC1} (c) Terminal 2 DC voltage V_{DC2}, (d) Terminal 2 DC current I_{DC2} .

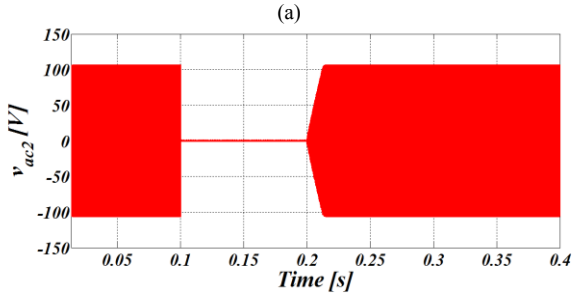
The converter DC waveforms are illustrated in Fig. 4. Fig. 4 (a) shows the DC voltage V_{DC1} dropping to zero due to the short circuit fault between t=0.1 and t=0.2. The pre-fault current I_{DC1} of the faulted bridge is negative in Fig. 4(b), since it is sinking power, dropping to zero during the fault. The results for non-faulted HV Bridge, V_{DC2} and I_{DC2} are depicted in Fig.4 (c) and (d). Observe that voltage V_{DC2} remains unchanged while current I_{DC2} dips to almost zero during the fault. After the fault is cleared, the converter fully recovers to its pre-fault operation status. Results show the DC fault is isolated as the non-faulted DC side current I_{DC2} is near zero. This confirms that no external DC circuit breakers are required. Reactive current is circulating inside the converter AC circuit but not contributing to power transfer nor overheating IGBTs.

B. DC fault on HV side (V_{DC2})

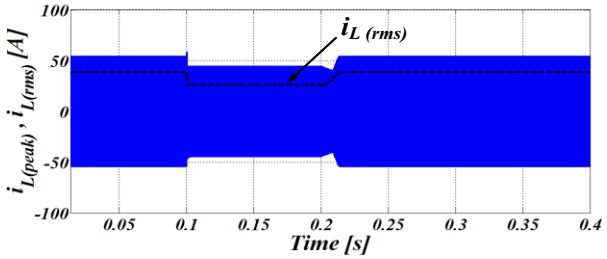
A zero impedance fault is also applied at the high voltage DC terminal of the converter. Prior to the fault, the converter is operating at full rated power with low voltage side sourcing power. The steady state AC and DC simulations results obtained are both shown in Fig. 5 and Fig. 6, for a DC fault applied between time *t=0.1s* and *t=0.2s*. It can be seen in Fig.5 (a) and (b) that the faulted bridge 2 AC voltage v_{ac2} drops to zero whilst, non-faulted bridge v_{ac1} voltage remains unchanged. Notice, the result shown for the inductor peak and RMS currents in Fig. 5 (c), further confirms fault current limiting capability of the DAB converter. Results can also be explained by the fact that the non-faulted bridge 2 views the fault on the other side as an AC fault, rather than DC and it is known that voltage-source converters are tolerant to AC faults. The DC sides voltage and current waveforms are demonstrated in Fig. 6. Bridge 1 DC voltage and current V_{DC1} and I_{DC1} are depicted in Fig.6 (a) and (b). Voltage V_{DC1} remains unchanged while average of current I_{DC1} is zero during the fault duration, thus no power transfer occurs. On the faulted bridge side, V_{DC2} and I_{DC2} (see Fig. 6 (c) and (d)) drop to zero. The converter recovers to pre-fault levels once the fault is cleared, further highlighting reliable fault isolation and recovery of the DAB converter.



(a)

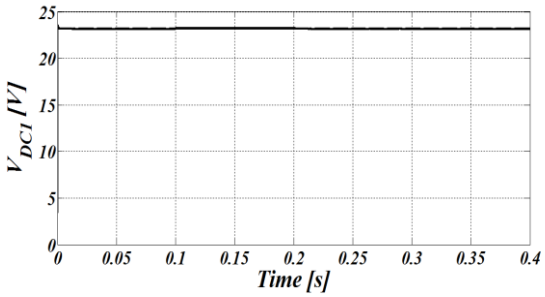


(b)

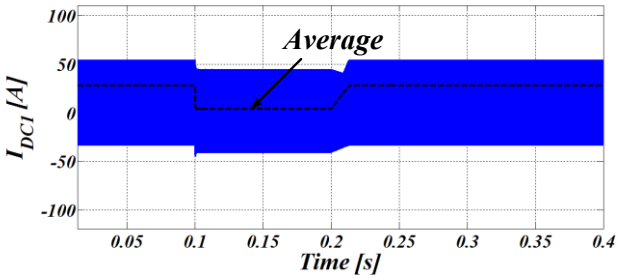


(c)

Fig. 5. Simulation results showing DC fault on HV side (a) Bridge 1 AC voltage v_{ac1}, (b) Bridge 2 AC voltage v_{ac2} , (c) Inductor current i_L.



(a)



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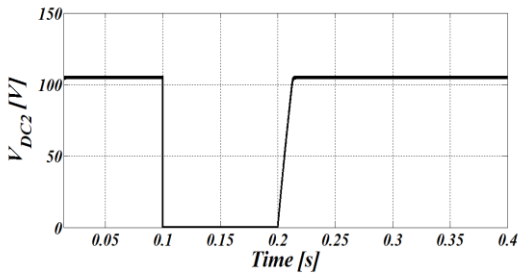
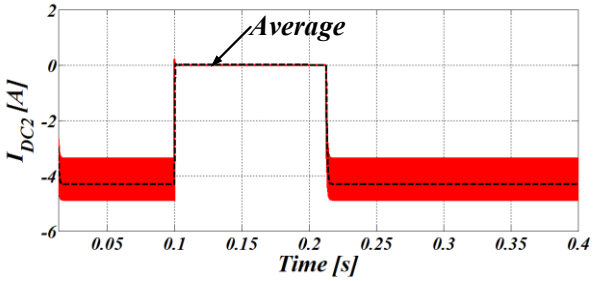


(c)



(d)

Fig. 6. Simulation results for DC voltages and currents for DC fault on HV side *(a)* Terminal 1 DC voltage V_{DC1}, (b) Terminal 1 DC current I_{DC1} (c) Terminal 2 DC voltage V_{DC2}, (d) Terminal 2 DC current I_{DC2} .

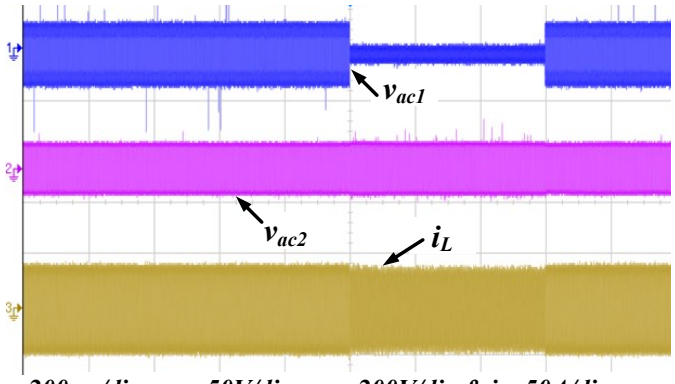
IV. EXPERIMETAL RESULTS

A. *DC fault on LV side* (V_{DC1})

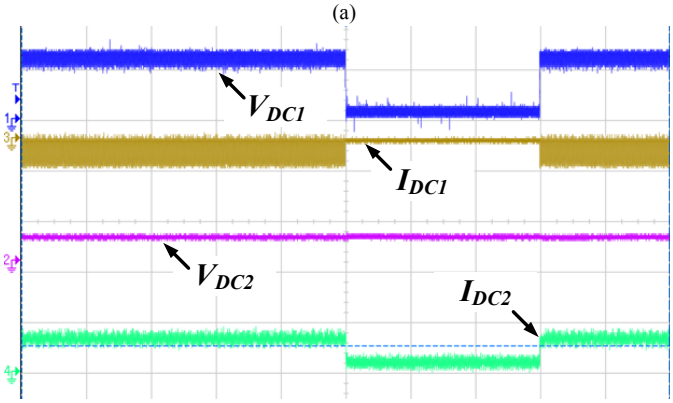
To further validate the theoretical analysis and simulations performed in sections II and III, an experimental DAB converter prototype, with parameters in Table I, was tested under fault conditions. Fig. 7 displays the experimental results obtained when the worst case short circuit fault was applied on the low voltage side (24V) of the prototype converter at full load. Bridge 2 is sourcing power to bridge 1.

Measured results show good resemblance to simulations in Fig. 3 and Fig. 4. In Fig. 7 (a), the AC waveforms of the converter are illustrated; from top to bottom, v_{ac1}, v_{ac2} and inductor/transformer current $i_{L.}$ Drop of faulted Bridge 1 voltage v_{ac1} to zero can be seen due to the fault, whereas v_{ac2} of bridge 2 remains unchanged.

The peak inductor current can be seen to remain fairly constant during the fault with no transient over currents during and after the fault is cleared. Measured DC variables in this study are shown in Fig. 7 (b); from top to bottom, V_{DC1}, I_{DC1}, V_{DC2} and I_{DC2}. Drop in V_{DC1} of the faulted Bridge 1 is evident whilst V_{DC2} remains unchanged when the short circuit fault is applied. The DC terminal currents I_{DC1} & I_{DC2}, both drop to zero during the fault duration. This is significant as it clearly verifies the converter inherent DC fault blocking capability. Once the fault is cleared, the pre-fault voltage and current levels are restored with no overvoltage or overcurrent transients.



(a)



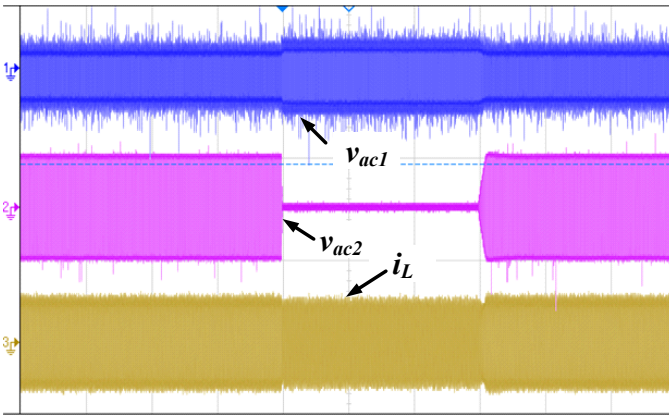
(b)

Fig. 7. Experimental waveforms showing short circuit DC fault on LV (24V) terminal (a) AC voltages and currents (b) DC voltages and currents

B. *DC fault on HV side* (V_{DC2})

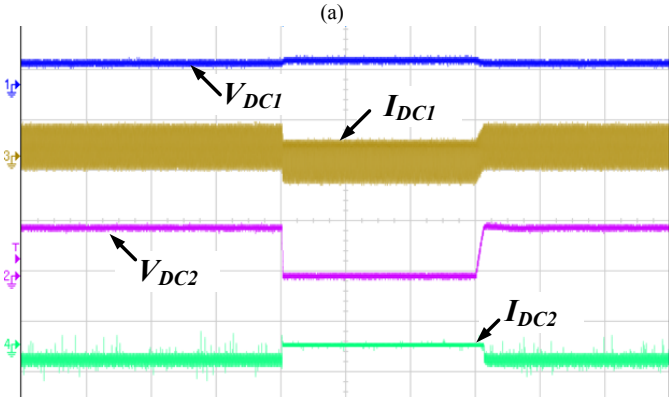
Short circuit fault was applied as well at the high voltage (100V) DC terminal of the experimental prototype converter. Results are shown in Fig. 8 (a) and (b) at full power rating with bridge 1 sourcing power to bridge 2. Similar to LV fault tests, it can be observed in Fig. 8 (a) that AC waveforms, v_{ac1}, $v_{ac2,}$ and i_L show good match with simulation results of Fig. 5. Particularly the peak fault current is fairly constant during the applied DC fault.

The measured DC voltage and current waveforms for both bridges are also depicted in Fig. 8(b); from top to bottom V_{DC1}, I_{DC1}, V_{DC2} and I_{DC2}. Comparing these measured results with the simulations of Fig. 6, a good matching of the converter fault response can be seen. It can be seen that, the DC voltage V_{DC2} during the fault plunges to zero whilst the non-faulted bridge 1 V_{DC1} voltage remains unchanged. The converter currents I_{DC1} and I_{DC2} both drop to zero during the fault, illustrating zero power transfer during the fault duration. Hence, this shows regardless of the location of fault, the converter response remains the same and the recovery to pre-fault levels is achieved.



200ms/div, v_{ac1}: 50V/div, v_{ac2} :100V/div & i_L :50A/div

(a)



200ms/div, V_{DC1}: 50V/div, I_{DC1} :100A/div,V_{DC2}: 100V/div, I_{DC2} :20A/div.

(b)

Fig. 8. Experimental waveforms showing short circuit DC fault on HV (100V) terminal (a) AC voltages and currents (b) DC voltages and currents

V. CONCLUSIONS

Dual Active Bridge (DAB) converter DC fault blocking property was investigated in this paper. It has been shown in simulation and experiments that when a DC fault is applied to one DC side, this is effectively seen by the counter bridge as an AC fault. Since voltage source converters are generally tolerant to AC side faults, the peak inductor/transformer current is the same as rated full-load peak current during the DC fault and RMS current reduces. This means DAB converter IGBTS do not need to be over-rated and can be continuously operated during the fault without the need to trip. No power transfer occurs since the AC current is mainly reactive and is circulating inside the converter causing both DC terminal currents to drop to zero during the fault, hence the inherent converter fault blocking property which does not require any controller action to interrupt fault current path. Analytical expressions have been verified by simulation and experimental results, which show that DAB DC-DC converter, can be considered as a reliable candidate for future DC transmission grids.

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